IN THE SPECIFICATION:

Please amend the paragraph beginning at page 1, line 11 as follows:

Since the main purpose of the flash memory's cell is to retain electrons for recording the desired information, it is considerably important ~~for~~ to be able to maintain a long span of charge retention. Generally, the electrons will be lost due to the ~~worst~~ failure of the electrical insulating layer over the flash memory's cell. Especially, it is the key point of charge retention whether the electrical insulating layer has a good insulating characteristic with respect to silicon-oxide layer on the bit lines. The conventional method for fabricating an electrical insulating layer on the flash memory's cell is shown in ~~FIG.~~ FIGS. 1-3.

Please amend the paragraph beginning at page 1, line 19 as follows:

Referring to FIG. 1, a polysilicon layer 102, a silicon nitride layer 104 and a cap layer 106 are sequentially formed on a gate region of a semiconductor substrate 100. Thereafter, a lithography and etching process is used to form spacing 110 between gate stacks 108. The silicon-oxide is filled into the spacer 110 by using a chemical vapor deposition (CVD) process. Since the structure of the silicon-oxide layer 112 formed by CVD process is undulated with the spacing 110, the top surface of the silicon-oxide layer 112 between the spacer 110 has a recess 114a.

Please amend the paragraph beginning at page 2, line 1 as follows:

Referring to FIG. 2, an etch back or chemical mechanical polishing (CMP) process is carried out to remove the silicon-oxide layer's 112 recess 114a. The silicon

nitride layer 104 serves as a stop layer so that the silicon-oxide is left inside spacing 110 to form a spacing silicon-oxide layer 116. According to the foregoing, since the top surface of silicon-oxide layer 112 is undulated with spacing 110, the so-called conformity, the surface of the spacing silicon-oxide layer 116 must still keep a ~~recess~~ recessed profile after an etch back. If the CMP process is used to remove the redundant silicon-oxide, the spacing silicon-oxide layer 116 also forms a recess 114b due to dish effect. Finally, referring FIG. 3, while a silicon nitride layer 104 is removed ~~away~~, the recess 114b is generated on the surface of the spacing silicon-oxide layer 116.

Please amend the paragraph beginning at page 2, line 11 as follows:

However, the recess 114b on the surface of the spacing silicon-oxide layer 116 has many disadvantages. The effective thickness 118 of the spacing silicon-oxide layer 114 is not enough to block a great deal of the impact of electrons ~~impact~~ but to severely destroy the bit lines (not shown in the figure) located under the spacing silicon-oxide layer 116. Additionally, the tip 120 portion of the spacing silicon-oxide layer 116 will cause the film a to crack when a deposition process is performed continuously. Further, after the silicon nitride 104 is removed, the step height between the polysilicon layer 102 and the spacing silicon-oxide layer 116 is too high so that the over-etching must be greatly increased but etching tolerance is inadequate resulting in the thin film's damage.

Please amend the paragraph beginning at page 3, line 2 as follows:

As a result, the primary object of the present invention ~~forms~~ is to form a dielectric layer and a planarized layer, and adjusts the etching rate ratio between the dielectric layer and the planarized layer for generating the spacing dielectric layer, such as silicon-oxide, ~~layer~~ having a round top and slant sides to benefit the following processes.

Please amend the paragraph beginning at page 3, line 6 as follows:

Another object of the present invention is to increase the effective thickness of the spacing of the silicon-oxide layer for blocking the bit lines from an ion implantation process.

Please amend the paragraph beginning at page 3, line 9 as follows:

According to the above objects, the present invention sets forth a method for forming an electric insulating layer on bit lines of the flash memory. First, a plurality of gate stacks are sequentially formed on the gate region of a semiconductor substrate wherein each of the gate stacks has a conductive layer, a mask layer and a cap layer, and the gate stacks are etched to form a plurality of spacing. Afterwards, a dielectric layer is formed on the semiconductor substrate to cover the gate stacks and then to fill ~~into~~ the spacing, and the dielectric layer is higher than the cap layer. A planarized layer is then formed on the dielectric layer to create a planar surface.

Please amend the paragraph beginning at page 3, line 17 as follows:

One etching step is utilized to entirely remove the dielectric layer located on the cap layer and thus spacing dielectric layer is formed inside the spacing. Afterwards, another etching step is used to remove the cap layer wherein the etching rate of the dielectric layer is less than that of the mask layer so that the spacing dielectric layer has a round top and slant sides to prevent a thin film of the following process from stress concentration. Finally, the mask layer is stripped and then the spacing silicon-oxide layer remains to form the electrical insulating layer on bit lines of the flash memory.

Please amend the paragraph beginning at page 4, line 6 as follows:

~~FIG.~~ FIGS. 1-3 illustrate cross-sectional views of a conventional process for fabricating an electrical insulating layer; and

Please amend the paragraph beginning at page 4, line 8 as follows:

~~FIG.~~ FIGS. 4-9 illustrate cross-sectional views of a process for fabricating an electrical insulating layer on bit lines of the flash memory according to the present invention.

Please amend the paragraph beginning at page 4, line 12 as follows:

The present invention is directed to a method for forming an electrical insulating layer on bit lines of the flash memory to improve the shortcomings of the prior art.

Please amend the paragraph beginning at page 4, line 22 as follows:

Still referring to FIG. 4, a dielectric layer 212 is formed on the semiconductor substrate 200, and then the gate stacks 208 are completely capped and the spacing 210 are filled into the dielectric layer 212. Further, the surface of the dielectric layer 212 is higher than that of the cap layer 206. Afterwards, a planarized layer 214 is formed on the dielectric layer 212 to create a planar surface. In the preferred embodiment of the present invention, the material of dielectric layer 212 is silicon-oxide formed by high-density plasma chemical vapor deposition (HDPCVD). The planarized layer 214 is a kind of organic material which is melted or ~~dissolve~~ dissolved in solvent, a liquid-filled solution, and is uniformly spread onto the dielectric layer 212 by surface tension of the solution.

Please amend the paragraph beginning at page 5, line 24 as follows:

Referring to FIG. 7, a second etching step is carried out to totally remove a portion of the dielectric layer 212 over the cap layer 206 and then a spacing dielectric layer 216 remains inside the spacing 210. The etching rate of the dielectric layer is preferably higher than that of the cap layer 206 during the second etching step. In the preferred embodiment of the present invention, a dry etching process is performed, and the etching rate ratio between the dielectric layer 212 and the cap layer 206 has a range from 1 to 10. The more preferred etch rate ratio has a range between 1.1 and 4.0. The mixed gas of CHF_3, CF_4 and Ar is used to etch the dielectric layer 212 on the cap layer 206.

Please amend the paragraph beginning at page 6, line 8 as follows:

Referring to FIG. 8, a third etching step is carried out to totally remove the cap layer 206. The etching rate of the dielectric layer 212 is less than that of the mask layer 204 during the third etching step so that the spacing dielectric layer 216 has a round top 218 and slant sides 220. In the preferred embodiment of the present invention, a dry etching process is performed ~~by~~ using CH_3F, O_2, Ar as etching gas, and the etching rate ratio between the dielectric layer 212 and the mask layer 204 has a range from 0 and 1. The more preferred etch rate ratio has a range between 0.1 and 0.5.

Please amend the paragraph beginning at page 6, line 15 as follows:

The round top 218 of the spacing dielectric layer 216 is capable of preventing the later film deposition from stress concentration, and the slant sides 220 can easily avoid cracking a think film. Furthermore, the effective thickness 222 of the spacing dielectric layer 216 is higher than that of the conventional process. In other ~~word~~ words, the spacing dielectric layer 216 is able to sufficiently block the electron impact and retains the dopant distribution within the bit lines. The slant sides 220 of the spacing dielectric layer 216 will reduce the thickness difference between the spacing dielectric layer 216 and the conductive layer 202 to form a preferred height so that an additional over-etching is not ~~need~~ needed for the later deposition process.

Please amend the paragraph beginning at page 6, line 24 as follows:

Referring to FIG. 9, the mask layer 204 is removed ~~away~~ and thus the spacing dielectric layer 216 is left. If the mask layer 204 is the material of silicon nitride, the H_3PO_4 may act as an etchant to remove the silicon nitride.

Please amend the paragraph beginning at page 7, line 2 as follows:

According to the ~~above-mentioned~~ discussion above, the present invention provides many advantages of forming electrical insulating layer on bit lines of the flash memory. For example, during the etch back and CMP process of the planarized layer 214, the conventional recess profile of the spacing dielectric layer 216 is preferably transformed into a round top 218 and slant sides 220 to prevent a later film deposition from ~~a crack~~ cracking. Additionally, the step height between spacing dielectric layer 216 and conductive layer 202 will not become bigger with respect to the effective thickness 222, so it is not ~~need~~ needed to increase the over-etching tolerance.

Please amend the paragraph beginning at page 7, line 10 as follows:

As understood by a person skilled in the art, the foregoing preferred embodiments of the present invention are illustrations rather than limitations of the present invention. ~~It is~~ They are intended to cover various modifications and similar arrangements included within the spirit and scope of the appended claims, the scope of which should be accorded the broadest interpretation so as to encompass all such modifications and similar ~~structure~~ structures.